

FIG. 1

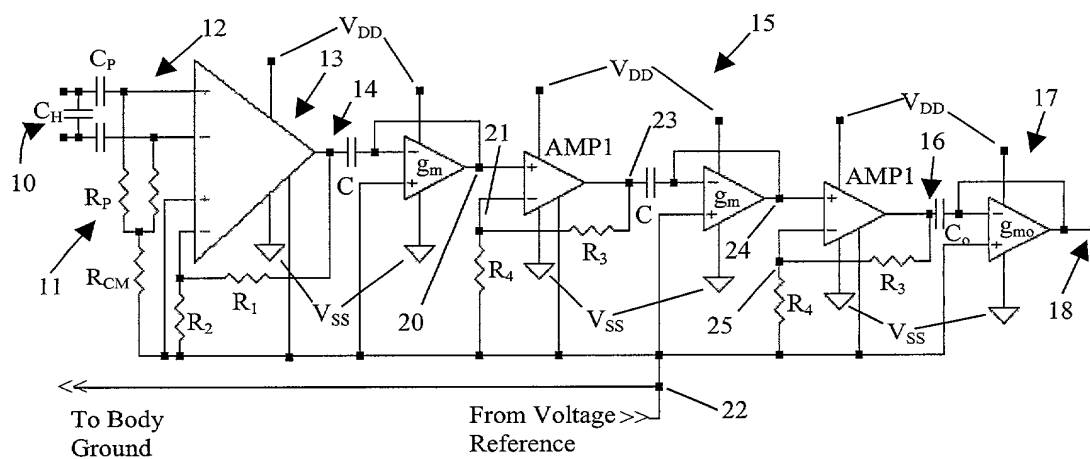


FIG. 2a

The diagram illustrates a multi-stage CMOS amplifier circuit. It begins with an input stage (10) featuring a differential pair of PMOS transistors (12, 13) and NMOS transistors (14, 15). The PMOS gates are connected to V_{DD} , and the NMOS gates are connected to V_{SS} . The input nodes are biased with a tail current source (11) consisting of a resistor R_B and a capacitor C_B connected to body ground. The output of the first stage is taken from node 20, which is connected to V_{SS} through resistor R_1 . This output is fed into the non-inverting input of the first amplifier stage (AMP1, 21). The output of AMP1 (23) is connected to V_{DD} through resistor R_3 and to the non-inverting input of a second amplifier stage (AMP1, 24) through a coupling capacitor C . The output of the second stage (25) is connected to V_{SS} through resistor R_4 and to the non-inverting input of a third amplifier stage (AMP1, 16) through another coupling capacitor C . The output of the third stage (17) is connected to V_{DD} through resistor R_3 and to the non-inverting input of a final output stage (18) through a coupling capacitor C_o . The output stage (18) consists of a PMOS transistor (17) and an NMOS transistor (18) with a transconductance g_{m0} . The output node is connected to V_{SS} through resistor R_4 . The entire circuit is powered by V_{DD} and V_{SS} rails.

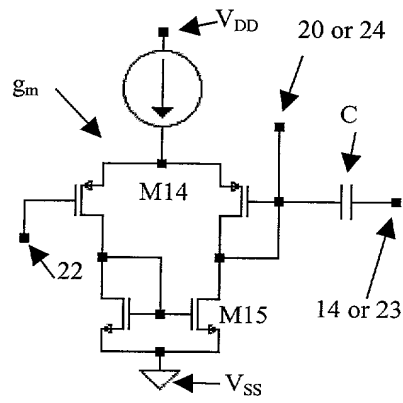


FIG. 4

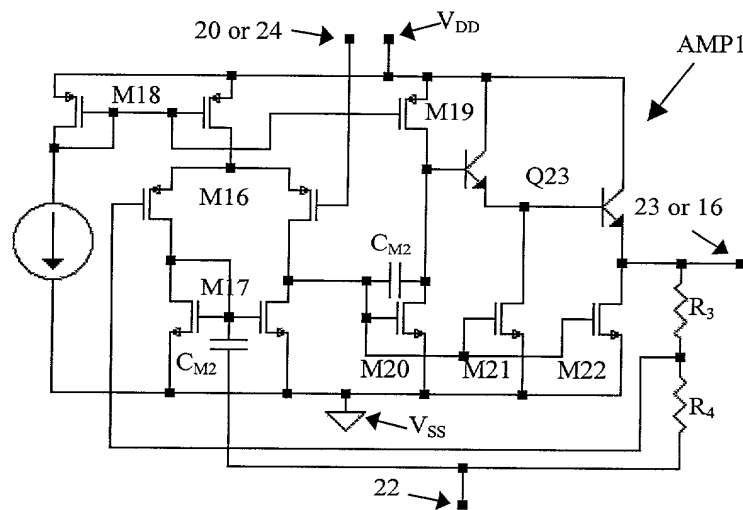


FIG. 5

